PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-244464
(43)Date of publication of application : 07.09.2001

(51)Int.Cl. H01L 29/786

(21)Application number : 2000-057440
(22)Date of filing : 02.03.2000

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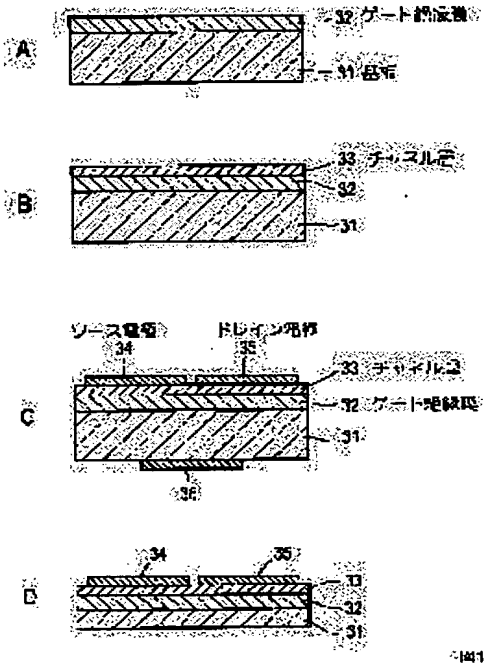
(54) METHOD OF MANUFACTURING METAL OXIDE TRANSISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To manufacture an FET by using a metal oxide semiconductor.
SOLUTION: A gate insulating film 32 of SiO2 is formed on an Si substrate 31. Zn(OAc)2.4H2O is suspended in isopropanol and the gate insulating film 32 is coated with this suspension. A channel layer 33 of ZnO is formed by thermal treatment and a source electrode 34 and a drain electrode 35 are formed thereon.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19)日本国特許庁(JP)　(12)公開特許公報（A）　(11)特許出願公開番号

特開２００１－２４４４６４
（Ｐ２００１－２４４４６４Ａ）
(43)公開日　平成13年9月7日(2001.9.7)

(51)Int.Cl.⁷	識別記号	ＦＩ			テーマコード(参考)
Ｈ０１Ｌ 29/786		Ｈ０１Ｌ	29/78	６１８　Ｂ	5F110

審査請求　未請求　請求項の数２　ＯＬ　（全５頁）

(21)出願番号　特願2000-57440(P2000-57440)

(22)出願日　平成12年3月2日(2000.3.2)

特許法第30条第1項適用申請有り　2000年1月18日～1月19日　日本セラミックス協会基礎科学部会主催の「第38回セラミックス基礎科学討論会　講演要旨集」において文書をもって発表

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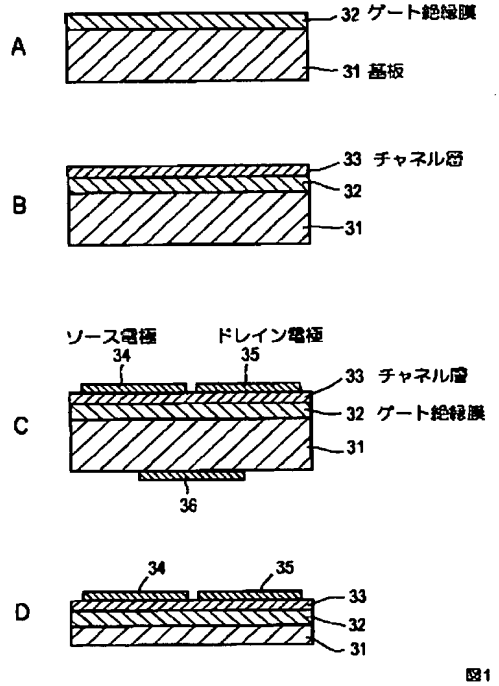
(54)【発明の名称】金属酸化物トランジスタの製造方法

(57)【要約】
【課題】　金属酸化物半導体を用いてＦＥＴを作製する。
【解決手段】　Ｓｉ基板３１上にＳｉO_2膜のゲート絶縁膜３２を形成し、Ｚｎ（ＯＡｃ）$_2$・４H_2Ｏをイソプロパノールに懸濁し、これをゲート絶縁膜３２上にコーティングした後、加熱処理してＺｎＯからなるチャネル層３３を形成し、その上にソース電極３４とドレイン電極３５を形成する。



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【特許請求の範囲】

【請求項１】　基板上にゲート絶縁膜を形成し、
そのゲート絶縁膜上にｎ形又はｐ形金属酸化物半導体薄膜を溶液法で作ってチャネル層を形成し、
そのチャネル層上にソース電極及びドレイン電極を形成することを特徴とする金属酸化物トランジスタの製造方法。

【請求項２】　上記溶液法によるチャネル層の形成は、上記金属酸化物が析出できる範囲で比較的低い温度で上記金属酸化物層を形成し、その後、上記温度より高い温度で上記金属酸化物を酸化させて上記金属酸化物半導体薄膜を得ることを特徴とする請求項１記載の金属酸化物トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は金属酸化物半導体を用いて金属－絶縁膜－半導体構造の電界効果形トランジスタを製造する方法に関する。

【０００２】

【従来の技術】従来のトランジスタは単結晶シリコンに不純物を拡散させ気相成長させたり、あるいは化合物半導体を気相成長させてｐ－ｎ接合を形成して製造するものが主流である。これらの場合は排ガスの処理に大きな設備と、処理費用を要した。一方、ゾル－ゲル（Ｓｏｌ－Ｇｅｌ）法に代表される溶液法により金属酸化物半導体を作製すれば排ガス処理の問題がなく、比較的簡単な設備で安価に作ることが可能である。しかし酸化物半導体は、一般に移動度が低いため、Ｓｉ、Ｇｅ、化合物半導体と比較して扱いにくい欠点があった。またゾル－ゲル法によって作製された薄膜はポーラスであることが多く、ガスセンサのように膜表面での吸着反応を利用することは試みられているが、厚さ方向の電導現象はほとんど利用されていない。

【０００３】例えば図５に示すように基板１１上に、ＮｉＯなどのｎ形金属酸化物層１２を形成し、その上にＴｉＯなどのｐ形金属酸化物層１３を溶液法により形成し、更にその上にＮｉＯなどのｎ形金属酸化物層１４を溶液法により形成して接合形トランジスタを構成することが考えられる。しかし各金属酸化物層の形成ごとに、６００～８００℃程度の高温加熱を必要とするため、ｐ形金属酸化物層１３を形成する際に、その下のｎ形金属酸化物層１２とｐ形金属酸化物層１３との境界に両層の複合酸化物膜１５が生成され、またｎ形金属酸化物層１４を形成する際にそのｎ形金属酸化物層１４とｐ形金属酸化物層１３との境界に両層の複合酸化物膜１６が生成され、しかも先に形成された複合酸化物膜１５が成長して、その膜厚が厚くなる。この複合酸化物膜、特に１５が完全な絶縁物となり、電子や正孔が移動することができず、トランジスタとして作用させることが困難である。

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【０００４】あるいは図６に示すように、シリコン基板１１上にＮｉＯのようなｎ形金属酸化層よりなるチャネル層１７を溶液法により形成し、そのチャネル層１７上の一部にSiO_2などのゲート絶縁膜１８を溶液法により形成し、ゲート絶縁膜１８上にゲート電極１９を、ゲート絶縁膜１８の両側においてチャネル層１７上にソース電極２１、ドレイン電極２２を形成して、Ｍ－Ｉ－Ｓ構造の電界効果形トランジスタを構成することも考えられる。この場合は、ゲート絶縁膜１８の形成後に、高温に加熱することがないため、チャネル層１７とゲート絶縁膜１８の境界に生じる複合酸化物膜はそれ程厚いものにはならない。しかし、チャネル層１７上に、ゲート絶縁膜１８を溶液法で作る場合、絶縁性の良好なものを作ることが困難であった。

【０００５】

【発明が解決しようとする課題】以上述べたように、溶液法により金属酸化物半導体を作製すれば製造設備が比較的簡単な半導体素子を作ることができるが、従来においてはトランジスタを作ることが困難であった。

【０００６】

【課題を解決するための手段】この発明によれば基板上にゲート絶縁膜を形成し、そのゲート絶縁膜上にｎ形又はｐ形金属酸化物半導体薄膜を溶液法で作ってチャネル層を形成し、そのチャネル層上にソース電極及びドレイン電極を形成する。上記溶液法によるチャネル層の形成は、比較的低い温度で金属酸化物を析出させた後、その温度より高い温度で析出した金属酸化物を酸化させて金属酸化物半導体薄膜を得ることが好ましい。

【０００７】

【発明の実施の形態】図１にこの発明の実施例を示す。先ず例えば（１００）単結晶シリコン（ｎ形、１．４×$10^{-2}\Omega cm$）の基板３１を用意し、その基板３１上にゲート絶縁膜３２を形成する。このゲート絶縁膜３２は基板３１を熱酸化してSiO_2膜を形成して作ることができる。あるいはスパッタリングによりSiO_2膜を形成してもよい。ゲート絶縁膜３２の厚さは例えば１３０ｎｍとする。

【０００８】このゲート絶縁膜３２上にｎ形又はｐ形の金属酸化物半導体薄膜を溶液法により形成してチャネル層３３とする（図１Ｂ）。例えば有機金属液体として$Zn(OAc)_2 \cdot 4H_2O$を用い、これをイソプロパノール（アルコールの一種）に懸濁させ、Ｚｎに対し等モルのジエタノールアミンを加水分解抑止剤として添加して溶解し、更に２倍モルの水を添加して０．４ｍｏｌ／１の溶液を調整する。この溶液をディップコーティング法、又はスプレイ法、スピンコーティング法によりゲート絶縁膜３２上にコーティングする。ディップコーティングの場合、溶液中から６ｃｍ／分の引き上げ速度で基板３１を引き上げると１回のコーティングで２０ｎｍのＺｎＯ膜が形成されるが、例えばＺｎＯの膜厚、つまり

チャネル層３３の膜厚が４０ｎｍになるようにコーティングを行い、その後、６００℃～９００℃の温度で空気中又は酸素雰囲気中で加熱処理を行い、ＺｎＯの膜、つまりチャネル層３３を形成する。

【０００９】次に図１Ｃに示すように、チャネル層３３上に金属膜により、ソース電極３４とドレイン電極３５を形成して電界効果形トランジスタ（ＦＥＴ）を得る。必要に応じて基板３１のゲート絶縁膜３２と反対側にゲート電極３６を形成する。基板３１自体をゲート電極としてもよい。電極３４，３５，３６は例えばＡｕの蒸着により、或いはＩＴＯ（インジウム、スズ酸化膜）などの透明電極材の溶液法により形成する。

【００１０】ゲート絶縁膜３２の厚さは、ゲート絶縁膜３２とチャネル層３３との境界に複合酸化膜が生成される点から、１００ｎｍ程度以上が好ましいが、チャネル制御が確実に行われる点から５００ｎｍ以下がよい。チャネルはチャネル層３３のゲート絶縁膜３２と接して形成され、ソース電極３４とドレイン電極３５の間にこのチャネルを通って電流が流れるには、電流はチャネル層３３の厚さ方向に流れて、電極からチャネルへまたチャネルから電極へ電流が流れることになる。この点からチャネル層３３の厚さを１００ｎｍ程度以上にすると、電子空乏層ができて電流が流れ難くなる。また１０ｎｍ程度以下にするとチャネルとしての動作が良好に行わなくなるおそれがある。これらの点からチャネル層３３の厚さは１０～１００ｎｍ程度がよい。

【００１１】チャネル層３３の形成時における加熱処理の温度を６００℃以下にすると、ゲート絶縁膜３２とチャネル層３３との境界にＺｎＯとＳｉO_2の複合酸化物膜Zn_2SiO_4が十分生成されないため、ゲート絶縁膜３２とチャネル層３３との密着性が悪くまたゲート絶縁膜３２を通るゲート電流が増加し、つまり絶縁性が悪く、良好なトランジスタ特性は得難くなる。従って、加熱処理温度は６００℃以上とする。一方加熱処理温度を９００℃以上にすると、複合酸化物膜Zn_2SiO_4の厚さが厚くなり、ＺｎＯ（チャネル層３３）の厚さが薄くなり過ぎ、ソース電極３４とドレイン電極３５間に電流が流れ難くなり、トランジスタ特性が得られなくなる。この点より酸化処理温度は９００℃以下とする。

【００１２】前記Ｚｎ（ＯＡｃ）$_2$・$4H_2O$を用いて作った、０．４ｍｏｌ／ｌのディップ溶液に、２回ディップコーティングし、６００℃、７００℃、８００℃及び９００℃でそれぞれ加熱処理を各６０分行ってＦＥＴを作製した。ここで６００℃で加熱処理とは、１回ディップコーティングを行い乾燥後６００℃で３０分間加熱処理を行い、再び１回ディップコーティングを行い乾燥後６００℃で３０分間加熱処理を行うことである。７００℃、８００℃及び９００℃での各加熱処理も同様にして各３０分間の加熱処理を２回行った。このようにして作製したＦＥＴのＸ線回折パターンを図２に示す。加熱処理の温度が低い６００℃ではZn_2SiO_4に基づくピークが確認できないが、ＺｎＯに基づくピークは確認される。加熱処理温度が高くなるに従ってZn_2SiO_4に基づくピークが確認できるようになり、逆にＺｎＯに基づくピークが小さくなり、９００℃ではZn_2SiO_4に基づくピークが可成り大きく現われ、逆にＺｎＯに基づくピークが可成り小さくなり、（１００）ＺｎＯに基づくピークはほぼなくなっている。

【００１３】これら実験結果より、加熱処理を、ＺｎＯを析出させるが、Zn_2SiO_4の生成を生じない低い温度、つまり６００℃による加熱を行ってＺｎＯを析出させ、結晶化させた後、９００℃で加熱処理して、結晶化したＺｎＯをSiO_2（ゲート絶縁膜）と反応させてZn_2SiO_4を薄く生成した。両加熱処理の合計時間を６０分とした。この場合のサンプルのＸ線回折パターンは、Zn_2SiO_4に基づくピークの温度が、９００℃のみで加熱処理した場合のそれよりも小さくなった。更に透過形電子顕微鏡により断面を観察した所、ＺｎＯとZn_2SiO_4との明白な界面が観察でき、SiO_2，Zn_2SiO_4及びＺｎＯの各膜厚はそれぞれ１１５．４０及び４５ｎｍであった。Zn_2SiO_4とSiO_2との界面は非常に密着性が良いものとなっていることも確認された。

【００１４】以上のことから加熱処理は酸化物半導体結晶が析出するが、その酸化物半導体結晶とゲート絶縁膜と反応しない温度で加熱し、酸化物半導体を析出結晶化させた後、これよりも高い温度で加熱して析出結晶化した半導体とゲート絶縁膜とを反応させる手法が好ましいことが理解される。２回ディップコーティングで各６００℃１０分の加熱処理と、９００℃１５分の加熱処理との合計３５分の加熱処理を行って作製したＺｎＯ－ＦＥＴのドレイン電流とゲート電流のゲート電圧に対する特性を測定した。その結果を図３に実線と破線でそれぞれ示す。この図から、ゲート電極への漏れ（ゲート電流）は少なく、トランジスタ特性が得られていることが理解される。

【００１５】上述において基板３１としては石英ガラス、Al_2O_3など他の材料でもよい。またゲート絶縁膜３２としてはSi_3N_4、ＳｉＯＮなどを用いてもよい。更にチャネル層３３としては、ＺｎＯに限らず、TiO_2、ＢａＯ、ＴｉＢａＯなどを用いてもよく、またｎ形金属酸化物半導体のみならず、ＮｉＯ、CuO_2、Co_2O_3などのｐ形金属酸化物半導体を用いてもよい。なお図１Ｄに示すように基板３１を切削又は化学的エッチングにより、ゲート絶縁膜３２と反対側を削り、基板３１の厚さを例えば０．０５ｍｍ以下、つまり可視光が透過する程度以下にし、場合によっては全て除去し、ゲート絶縁膜３２にＩＴＯなどの透明電極（ゲート電極）を付けて液晶駆動トランジスタとして使用できるようにすることもできる。つまり透明なＦＥＴとするこ

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ともできる。また図４に示すように、図１Ｃに対し、ソース電極３４，ドレイン電極３５の形成面上に、これらの周縁部と一部重なるように酸化シリコンや強誘電体チタン酸バリウムなどの絶縁膜３７を形成してチャネル層表面を流れる洩れ電流を減らすように少なくともチャネル層膜上に絶縁膜を溶液法で形成することが好ましい。

【００１６】

【発明の効果】以上述べたようにこの発明によれば、チャネル層を溶液法により形成することにより、金属酸化物半導体をチャネル層としたＦＥＴを作製することができ、排ガス処理など大きな設備を必要とせず、比較的簡単な設備で製造することができる。

【図面の簡単な説明】

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【図１】この発明の実施例の製造工程を説明するための断面図。

【図２】各種加熱処理温度で作製したＺｎＯ－ＦＥＴのＸ線回折パターンを示す図。

【図３】この発明方法で作ったＺｎＯ－ＦＥＴのトランジスタ特性を示す図。

【図４】この発明方法で作られたトランジスタの例を示す断面図。

【図５】従来技術で考えられる接合形金属酸化物半導体トランジスタを示す断面図。

【図６】従来技術で考えられる金属酸化物半導体ＦＥＴを示す断面図。

【図１】

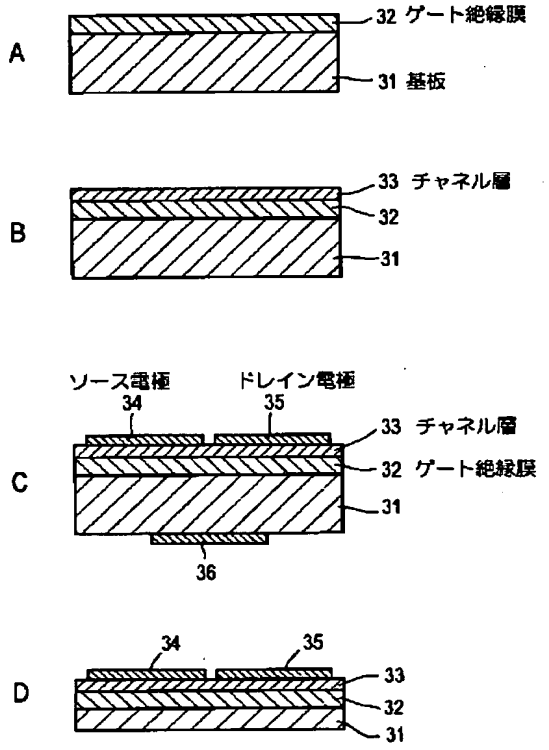

図1

【図２】

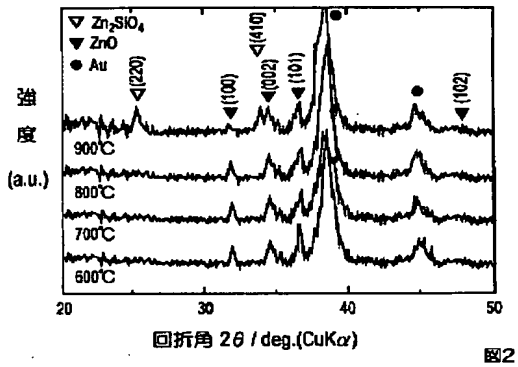

図2

【図３】

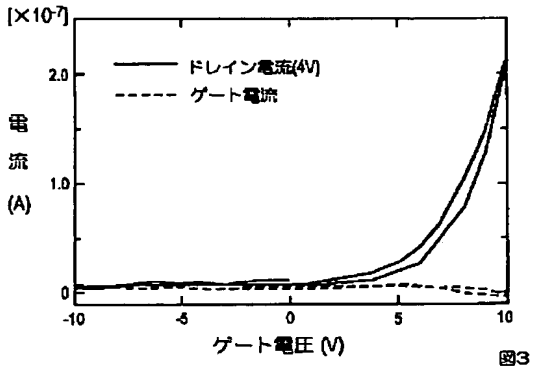

図3

【図４】

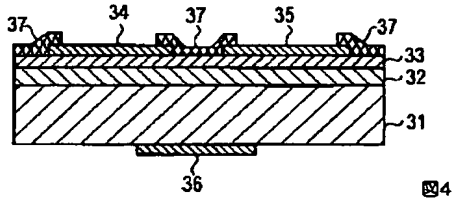

図4

【図５】

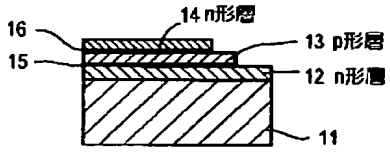

図5

【図６】

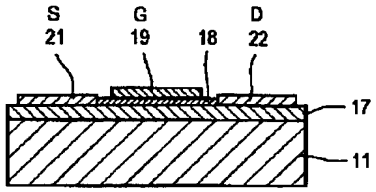

図6

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Ｆターム(参考)　5F110 DD01 DD03 DD05 DD13 FF03
FF04 GG01 GG04 GG25

Bibliography

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(19) [Publication country] Japan Patent Office (JP)
(12) [Kind of official gazette] Open patent official report (A)
(11) [Publication No.] JP, 2001-244464, A (P2001-244464A)
(43) [Date of Publication] September 7, Heisei 13 (2001. 9.7)
(54) [Title of the Invention] The manufacture approach of a metallic-oxide transistor
(51) [The 7th edition of International Patent Classification]
H01L 29/786
[FI]
H01L 29/78 618 B
[Request for Examination] Un-asking.
[The number of claims] 2
[Mode of Application] OL
[Number of Pages] 5
(21) [Application number] Application for patent 2000-57440 (P2000-57440)
(22) [Filing date] March 2, Heisei 12 (2000. 3.2)
[Indication of exceptions to lack of novelty] Those with the 1st term application application of Article 30 of Patent Law January 18, 2000 to January 19 In Ceramic Society of Japan fundamental science sectional meeting-sponsored "the collection of 38th ceramic fundamental science debate lecture summaries", it announces with a document.
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[Theme code (reference)]
5F110
[F term (reference)]
5F110 DD01 DD03 DD05 DD13 FF03 FF04 GG01 GG04 GG25

[Translation done.]

* NOTICES *

Epitome

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(57) [Abstract]
[Technical problem] FET is produced using a metal oxide semiconductor.
[Means for Solution] It is SiO2 on the Si substrate 31. Membranous gate dielectric film 32 is formed, after suspending Zn(OAc) 2 and 4H2 O in isopropanol and coating this on gate dielectric film 32, the channel layer 33 which heat-treats and consists of ZnO is formed, and the source electrode 34 and the drain electrode 35 are formed on it.

[Translation done.]

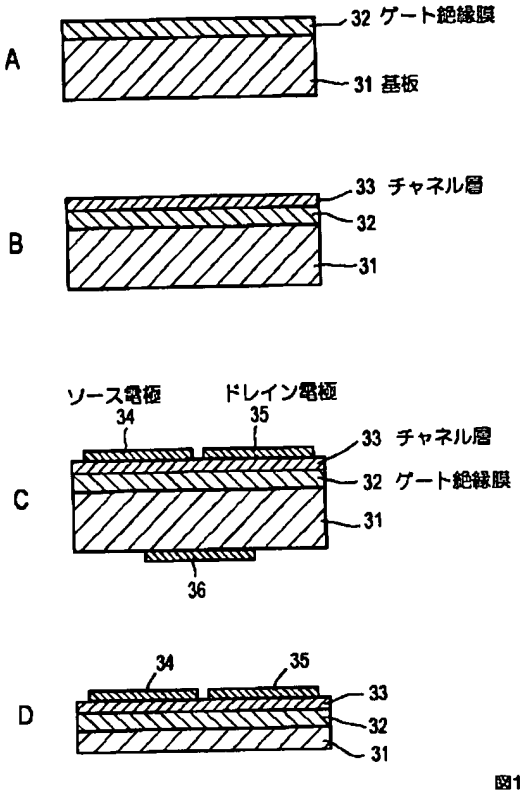


図1

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the metallic-oxide transistor characterized by forming gate dielectric film on a substrate, making n form or p form metal oxide semiconductor thin film with a solution

method, forming a channel layer on the gate dielectric film, and forming a source electrode and a drain electrode on the channel layer.
[Claim 2] Formation of the channel layer by the above-mentioned solution method is the manufacture approach of the metallic-oxide transistor according to claim 1 characterized by forming the above-mentioned metal oxide layer at comparatively low temperature in the range in which the above-mentioned metallic oxide can deposit, oxidizing the above-mentioned metallic oxide at temperature higher than the above-mentioned temperature after that, and obtaining the above-mentioned metal oxide semiconductor thin film.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the approach of manufacturing the field effect transistor of metal-insulator layer-semiconductor structure using a metal oxide semiconductor.
[0002]
[Description of the Prior Art] As for the conventional transistor, what single crystal silicon is made to diffuse an impurity, and is made to carry out vapor growth, or is made to carry out vapor growth of the compound semiconductor, and forms and manufactures p-n junction is in use. Processing of exhaust gas took a big facility and processing costs in these cases. on the other hand -- sol-gel (Sol-Gel) -- it is possible for there to be no problem of offgas treatment, if a metal oxide semiconductor is produced with the solution method represented by law, and to make cheaply with a comparatively easy facility. However, generally, since mobility was low, the oxide semiconductor had the fault

which is hard to treat as compared with Si, germanium, and a compound semiconductor. Moreover, although the thin film produced by the sol-gel method is porous in many cases and to use the adsorption reaction on the front face of the film like a gas sensor is tried, most electrical conduction phenomena of the thickness direction are not used.

[0003] For example, it is possible to form n form metal oxide layers 12, such as NiO, on a substrate 11, as shown in drawing 5 , to form p form metal oxide layers 13, such as TiO, with a solution method on it, to form n form metal oxide layers 14, such as NiO, with a solution method on it further, and to constitute a junction transistor. However, since about 600-800-degree C heating at high temperature is needed for every formation of each metal oxide layer, In case p form metal oxide layer 13 is formed, the multiple oxide film 15 of both layers is generated by the boundary of n form metal oxide layer 12 under it, and p form metal oxide layer 13. Moreover, in case n form metal oxide layer 14 is formed, the multiple oxide film 15 which the multiple oxide film 16 of both layers was generated by the boundary of the n form metal oxide layer 14 and p form metal oxide layer 13, and was moreover previously formed in it grows, and the thickness becomes thick. It is difficult for especially 15 to be unable to become this multiple oxide film and a perfect insulating material, and to be able to move neither in an electron nor an electron hole, but to make it act as a transistor.

[0004] or the channel layer 17 which consists of an n form metal oxidizing zone like NiO on a silicon substrate 11 as shown in drawing 6 -- a solution method -- forming -- the part on the channel layer 17 -- SiO2 etc. -- forming gate dielectric film 18 with a solution method, forming the source electrode 21 and the drain electrode 22 for the gate electrode 19 on the channel layer 17 in the both sides of gate dielectric film 18 on gate dielectric film 18, and constituting the field effect transistor of M-I-S structure is also considered. In this case, in order not to heat to an elevated temperature after formation of gate dielectric film 18, the multiple oxide film produced on the boundary of the channel layer 17 and gate dielectric film 18 will not become so thick. However, on the channel layer 17, when making gate dielectric film 18 with a solution method, it was difficult to make a good insulating thing.

[0005]

[Problem(s) to be Solved by the Invention] Although the manufacturing facility could make the comparatively easy semiconductor device when producing the metal oxide semiconductor with the solution method as stated above, it was difficult to make a transistor in the former.

[0006]
[Means for Solving the Problem] According to this invention, gate dielectric film is formed on a substrate, on that gate dielectric film, n form or p form metal oxide semiconductor thin film is made with a solution method, a channel layer is formed, and a source electrode and a drain electrode are formed on that channel layer. After formation of the channel layer by the above-mentioned solution method deposits a metallic oxide at comparatively low temperature, it is desirable to oxidize the metallic oxide which deposited at temperature higher than the temperature, and to obtain a metal oxide semiconductor thin film.
[0007]
[Embodiment of the Invention] The example of this invention is shown in drawing 1 . The substrate 31 of single crystal silicon (n form, 1.4x10-2ohmcm) is prepared first, for example (100), and gate dielectric film 32 is formed on the substrate 31. This gate dielectric film 32 oxidizes a substrate 31 thermally, and is SiO2. The film can be formed and made. Or it is SiO2 by sputtering. The film may be formed. Thickness of gate dielectric film 32 is set to 130nm.
[0008] The metal oxide semiconductor thin film of n form or p form is formed with a solution method on this gate dielectric film 32, and it considers as the channel layer 33 (drawing 1 B). for example, this is suspended in isopropanol (a kind of alcohol), using Zn(OAc) 2 and 4H2 O as an organic metal liquid -- making -- Zn -- receiving -- the diethanolamine of equimolar -- as a hydrolysis retardant -- adding -- dissolving -- further -- the water of 2 double mol is added and the solution of 0.4 mol/l is adjusted. This solution is coated on gate dielectric film 32 with a DIP coating method or a spray method, and a spin coating method. In the case of DIP coating, if a substrate 31 is pulled up at the raising rate for 6cm/out of a solution, the 20nm ZnO film will be formed by one coating, but coating is performed so that the thickness of ZnO, i.e., the thickness of the channel layer 33, may be set to 40nm, for example, and it heat-treats in air or an oxygen ambient atmosphere at the temperature of 600 degrees C - 900 degrees C after that, and forms, the film 33, i.e., the channel layer, of ZnO.
[0009] Next, as shown in drawing 1 C, on the channel layer 33, by the metal membrane, the source electrode 34 and the drain electrode 35 are formed, and a field effect transistor (FET) is obtained. The gate electrode 36 is formed in the gate dielectric film 32 and the opposite side of a substrate 31 if needed. It is good also considering substrate 31 the very thing as a gate electrode. electrodes 34, 35, and 36 -- for example, vacuum evaporationo of Au -- or it forms with the solution

method of transparent electrode material, such as ITO (an indium, stannic-acid-ized film).

[0010] The thickness of gate dielectric film 32 has good 500nm or less from the point that channel control is certainly performed from the point that a compound oxide film is generated by the boundary of gate dielectric film 32 and the channel layer 33 although about 100nm or more is desirable. In order to form a channel in contact with the gate dielectric film 32 of the channel layer 33 and for a current to flow through this channel between the source electrode 34 and the drain electrode 35, a current will flow in the thickness direction of the channel layer 33, and a current will flow from an electrode from a channel to an electrode to a channel again. If thickness of the channel layer 33 is set to about 100nm or more from this point, an electronic depletion layer will be made and a current will stop being able to flow easily. Moreover, when it is made about 10nm or less, there is a possibility that the actuation as a channel may stop carrying out good. The thickness of these points to the channel layer 33 has good about 10-100nm.

[0011] When temperature of the heat-treatment at the time of formation of the channel layer 33 is made into 600 degrees C or less, it is ZnO and SiO2 to the boundary of gate dielectric film 32 and the channel layer 33. Multiple oxide film Zn2 SiO4 Since it is not generated enough, the gate current by which the adhesion of gate dielectric film 32 and the channel layer 33 passes along gate dielectric film 32 bad again increases, that is, insulation is bad and good transistor characteristics become difficult to get. Therefore, heat-treatment temperature is made into 600 degrees C or more. On the other hand, when heat-treatment temperature is made into 900 degrees C or more, it is multiple oxide film Zn2 SiO4. Thickness becomes thick, the thickness of ZnO (channel layer 33) becomes thin too much, between the source electrode 34 and the drain electrode 35, a current stops being able to flow easily and transistor characteristics are no longer acquired. Oxidation-treatment temperature is made into 900 degrees C or less from this point.

[0012] In the DIP solution of 0.4 mol/l made using said Zn(OAc) 2 and 4H2 O, DIP coating was carried out twice and the line produced FET for heat-treatment 60 minute each, respectively at 600 degrees C, 700 degrees C, 800 degrees C, and 900 degrees C. Heat-treatment is performing DIP coating once, performing heat-treatment for 30 minutes at 600 degrees C after desiccation, performing DIP coating once again, and performing heat-treatment for 30 minutes at 600 degrees C after

desiccation at 600 degrees C here. Each heat-treatment at 700 degrees C, 800 degrees C, and 900 degrees C performed heat-treatment for 30 minutes each twice similarly. Thus, the X diffraction pattern of produced FET is shown in drawing 2 . At 600 degrees C with the low temperature of heat-treatment, it is Zn2 Si04. Although the based peak cannot be checked, the peak based on ZnO is checked. heat-treatment temperature becomes high -- alike -- following -- Zn2 Si04 the peak conversely based on [can check the based peak now and] ZnO -- small -- becoming -- 900 degrees C -- Zn2 Si04 the based peak -- ****** -- the peak conversely based on [appear greatly and] ZnO -- ****** -- it became small and the peak based on ZnO (100) is lost mostly.

[0013] Although heat-treatment deposits ZnO from these experimental results, it is Zn2 Si04. After performing the low temperature which does not produce generation, i.e., heating by 600 degrees C, depositing ZnO and making it crystallize, heat-treat at 900 degrees C and crystallized ZnO is made to react with Si02 (gate dielectric film), and it is Zn2 Si04. It generated thinly. Sum total time amount of both heat-treatment was made into 60 minutes. The X diffraction pattern of the sample in this case became smaller than it when the temperature of the peak based on Zn2 Si04 heat-treats only at 900 degrees C. Furthermore, the place, and ZnO and Zn2 Si04 which observed the cross section with the transmission electron microscope A clear interface can be observed and they are Si02 and Zn2 Si04. And each thickness of ZnO was 115.40 and 45nm, respectively. Zn2 Si04 Si02 As for the interface, it was also checked very much that it is what has good adhesion.

[0014] It is understood that the technique to which the above thing to heat-treatment makes the semi-conductor which heated and carried out deposit crystallization at temperature higher than this after heating at the oxide-semiconductor crystal and gate dielectric film, and the temperature which does not react and carrying out deposit crystallization of the oxide semiconductor, although the oxide-semiconductor crystal deposited, and gate dielectric film react is desirable. The property over the gate voltage of the drain current and gate current of ZnO-FET which performed heat-treatment for a total of 35 minutes of 600-degree-C each heat-treatment for 10 minutes, and 900-degree-C heat-treatment for 15 minutes by DIP coating twice, and was produced was measured. A continuous line and a broken line show the result to drawing 3 , respectively. There is little leakage (gate current) by the gate electrode from this drawing, and it is understood that transistor characteristics are acquired.

[0015] **** -- setting -- as a substrate 31 -- quartz glass and aluminum

203 etc. -- other ingredients are sufficient. Moreover, SiN4, SiON, etc. may be used as gate dielectric film 32. furthermore -- as the channel layer 33 -- not only ZnO but TiO2, BaO, TiBaO, etc. -- you may use -- moreover, not only n form metal oxide semiconductor but NiO and CuO2, and Co 203 etc. -- p form metal oxide semiconductor may be used. In addition, as shown in drawing 1 D, by cutting or chemical etching, a substrate 31 is shaved for gate dielectric film 32 and the opposite side, and it carries out to below extent to which 0.05mm or less, i.e., the light, penetrates the thickness of a substrate 31, all are removed depending on the case, transparent electrodes (gate electrode), such as ITO, are attached to gate dielectric film 32, and it can make it possible to use it as a liquid crystal drive transistor. That is, it can also be referred to as transparent FET. Moreover, as shown in drawing 4 , it is desirable to form an insulator layer with a solution method on a channel layer membrane at least so that the leak current which forms the insulator layers 37, such as silicon oxide and ferroelectric barium titanate, and flows a channel layer front face may be reduced so that it may lap with these periphery sections in part on the forming face of the source electrode 34 and the drain electrode 35 to drawing 1 C.

[0016]

[Effect of the Invention] As stated above, FET which used the metal oxide semiconductor as the channel layer by forming a channel layer with a solution method according to this invention can be produced, and big facilities, such as offgas treatment, are not needed, but it can manufacture with a comparatively easy facility.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view for explaining the production process of the example of this invention.
[Drawing 2] Drawing showing the X diffraction pattern of ZnO-FET produced at various heat-treatment temperature.
[Drawing 3] Drawing showing the transistor characteristics of ZnO-FET made by this invention approach.
[Drawing 4] The sectional view showing the example of the transistor made by this invention approach.
[Drawing 5] The sectional view showing the junction type metal oxide semiconductor transistor considered with the conventional technique.
[Drawing 6] The sectional view showing the metal oxide semiconductor FET considered with the conventional technique.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

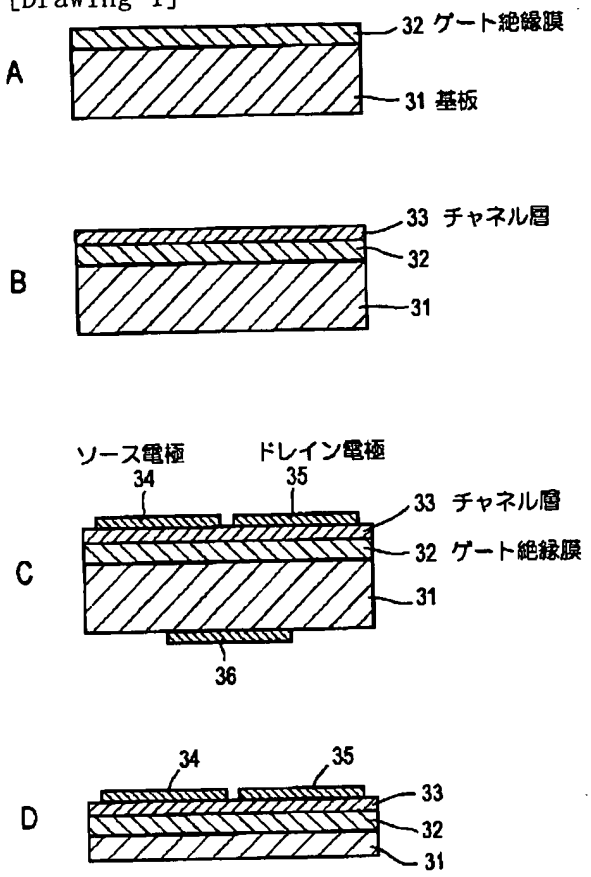


図1

[Drawing 2]

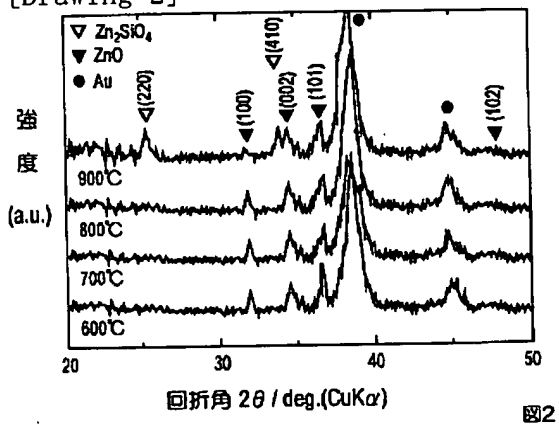


図2

[Drawing 3]

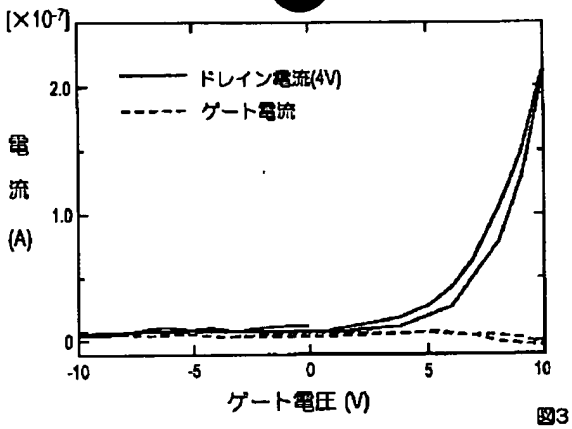
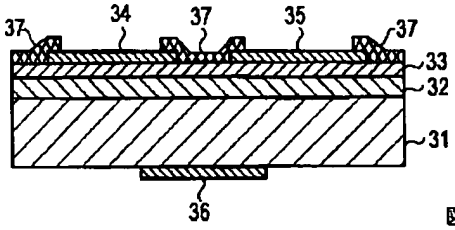


図3

[Drawing 4]



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[Drawing 5]

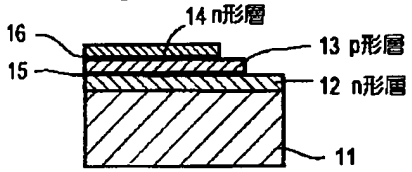

図5

[Drawing 6]

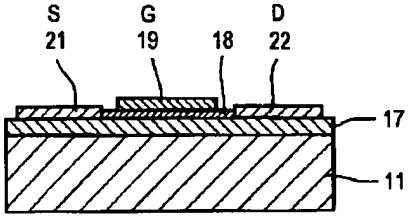

図6

[Translation done.]